Claims 1-11 (canceled)

Claim 12 (currently amended): A method for converting a C-type language program to a hardware design, comprising the steps of:

creating an algorithmic representation in a given C-type programming language corresponding to a preliminary hardware design;

compiling the C-type programming language preliminary hardware design into a hardware description language (HDL) synthesizable design, wherein the step of compiling comprises the steps of:

mapping predetermined C-type programming language expressions to functionally equivalent HDL program language expressions;

assigning input/output as defined in the C-type program to specific wires the HDL synthesizable design; and

~~The method of claim 7 wherein the step of compiling further comprises the step of~~

compiling C-type programming language structure assignment, structure function parameters, and structure function return values into HDL synthesizable expressions; and

configuring in the HDL synthesizable design an interface for a gate-level hardware representation.

Claims 13-22 (canceled)

Claim 23 (currently amended): A method for converting a C-type language program to a hardware design, comprising the steps of:

creating an algorithmic representation in a given C-type programming language corresponding to a preliminary hardware design;

compiling the C-type programming language preliminary hardware design into a hardware description language (HDL) synthesizable design, wherein the step of compiling comprises the steps of:

compiling a C-type program control flow into an HDL state machine; and

assigning input/output as defined in the C-type program to specific wires in the HDL synthesizable design;

configuring in the HDL synthesizable design an interface for the gate-level hardware representation; and

~~The method of claim 13, further comprising the step of~~

compiling C-type programming language structure assignment, structure function parameters, and structure function return values into HDL synthesizable expressions.

Claims 24-46 (canceled)

Claim 47 (currently amended): A method for converting a high-level language program to a hardware design, comprising the steps of:

creating an algorithmic representation in a given high-level programming language corresponding to a preliminary hardware design;

translating the high-level programming language preliminary hardware design into a C-type programming language preliminary hardware design;

compiling the C-type programming language preliminary hardware design into a hardware description language (HDL) synthesizable design, wherein the step of compiling comprises the steps of:

compiling a C-type program control flow into an HDL state machine; and

assigning input/output as defined in the C-type program to specific wires in the HDL synthesizable design;

configuring in the HDL synthesizable design an interface for the gate-level hardware representation; and

~~The method of claim 37, further comprising the step of~~

compiling C-type programming language structure assignment, structure function parameters, and structure function return values into HDL synthesizable expressions.

Claims 48-55 (canceled)